Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please cancel claims 14-39.

Listing of Claims:

1. (Original) A method of operating a DRAM device in either a high power, full density mode or a low power, half density low mode, comprising:

reordering each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address;

when operating in the full density mode, accessing rows of memory cells in an array according to the reordered row address;

when operating in the full density mode, refreshing the memory cells in the array at a first rate;

when operating in the half density mode, accessing rows of memory cells in the array according to the reordered row address, and, when accessing each row of memory cells, also accessing an adjacent row of memory cells;

when operating in the half density mode, refreshing memory cells in the memory array at a second rate that is slower than the first rate; and

when switching from operation in the full density mode to operation in the half density mode, transferring data from each row of the array in which data are stored to the adjacent row of memory cells.

2. (Original) The method of claim 1 wherein the act of transferring data from each row of the array to the adjacent row comprises:

activating a word line for the row thereby coupling each of the memory cells in the row to one of a respective pair of complimentary digit lines;

sensing the voltage between each of the complimentary pairs of digit lines using a respective sense amplifier that drives the differential voltage between the complimentary digit lines to a predetermined voltage; and

while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines, activating a word line for the adjacent row thereby coupling one of each of the pairs of complimentary digit lines to the respective memory cell in the adjacent row.

3. (Original) The method of claim 2 wherein the act of activating a word line comprises activating a word line for an even-numbered row, and wherein the act of activating a word line for a row adjacent the activated word line while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines comprises activating an odd-numbered word line for a row adjacent the even-numbered row having the activated word line.

4. (Original) The method of claim 1 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of accessing rows of memory cells in the array according to the reordered row address and accessing the adjacent row of memory cells comprises coupling a memory cell in each column of the accessed row of memory cells to the same digit line to which a memory cell in the same column of the adjacent row of memory cells is coupled.

5. (Original) The method of claim 1 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of accessing rows of memory cells in the array according to the reordered row address and accessing the adjacent row of memory cells comprises coupling a memory cell in each column of the accessed row of memory cells to a different digit line from which a memory cell in the same column of the adjacent row of memory cells is coupled.

6. (Original) A method of operating a DRAM device, comprising:

reordering each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address; and

accessing rows of memory cells in a memory array according to the reordered row address.

7. (Original) A method of operating a DRAM device in either a high power, full density mode or a low power, half density mode, comprising:

when operating in the full density mode, refreshing rows of memory cells in an array one-row-at-a-time at a first rate;

when operating in the half density mode, refreshing rows of memory cells in the array two-rows-at-a-time at a second rate that is slower than the first rate; and

when switching from operation in the full density mode to operation in the half density mode, transferring data from each row of the array in which data are stored to another row of memory cells.

8. (Original) The method of claim 7 wherein the act of transferring data from each row of the array in which data are stored to another row of memory cells comprises transferring data from each row of the array in which data are stored to a respective adjacent row of memory cells.

9. (Original) The method of claim 7 wherein the act of transferring data from each row of the array in which data are stored to another row of memory cells comprises:

activating a word line for the row in which data are stored thereby coupling each of the memory cells in the row to one of a pair of respective complimentary digit lines;

sensing the voltage between each of the pairs of complimentary digit lines using a respective sense amplifier that drives the differential voltage between the complimentary digit lines to a predetermined voltage; and

while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines, activating a word line for the another row of

memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the another row of memory cells.

10. (Original) The method of claim 9 wherein the act of activating a word line for the another row of memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the another row of memory cells comprises activating a word line for a respective adjacent row of memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the respective adjacent row of memory cells.

11. (Original) The method of claim 7 wherein the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously refreshing adjacent rows of memory cells.

12. (Original) The method of claim 7 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously coupling a memory cell in each column of one row of memory cells to the same digit line to which a memory cell in the same column of another row of memory cells is coupled.

13. (Original) The method of claim 7 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously coupling a memory cell in each column of one row of memory cells to a different digit line from which a memory cell in the same column of another row of memory cells is coupled.

Claims 14-39 (Cancelled)